CLAIMS

1. A method for maintaining an accurate frequency for a voltage controlled oscillator in a phase-locked loop, comprising the steps of:

receiving, at a phase detector, a phase input signal and a phase feedback signal from the voltage controlled oscillator;

measuring a pulse width property of an error signal output from the phase detector to obtain a pulse width property measurement;

storing the pulse width property measurement in a memory; and

generating a new signal based on the stored pulse width property measurement to maintain the frequency of the voltage controlled oscillator.

2. The method of claim 1, wherein the generating step is performed when the phase input signal is lost.

3. The method of claim 1, wherein the generating step is performed when the phase input signal becomes unsuitable for proper operation of the phase-locked loop.

4. The method of claim 1, wherein the measuring step is performed at periodic intervals.

5. The method of claim 1, wherein the measuring step is performed as an initial on-site calibration function.

6. The method of claim 1, wherein the phase input signal is derived from a reference clock signal.

7. The method of claim 1, wherein the pulse width property comprises a pulse width measurement of a high level of the error signal and a pulse width measurement of a low level of the error signal, and the measuring step further comprises the steps of:

detecting a first rising edge of the error signal;

starting a counter to measure the high level pulse width of the error signal;

detecting a falling edge of the error signal;

stopping the counter to obtain the high level pulse width;

restarting the counter to measure the low level pulse width of the error signal;

detecting a second rising edge of the error signal; and

stopping the counter to obtain the low level pulse width.

8. The method of claim 1, wherein the pulse width property measurement comprises a high pulse width measurement of a high level of the error signal and a pulse width measurement of a low level of the error signal, and the generating step further includes the steps of:

starting a count down counter from a count corresponding to the stored high level pulse width measurement;

generating a high level of the new signal until the counter stops;

restarting the counter to count down from a count corresponding to the stored low level pulse width measurement; and,

generating a low level of the new signal until the counter stops.

9. The method of claim 2, wherein upon a reappearance of the phase input signal, the generating step is terminated.

10. The method of claim 3, wherein upon acquiring a suitable phase input signal, the generating step is terminated.

11. A system comprising:

a phase detector that generates an error signal from a phase input signal and a phase feedback signal from a voltage controlled oscillator;

a measurement circuit operative to measure a pulse width property of the error signal;

a memory module for storing the measured pulse width property; and

a generation circuit operative to retrieve the measured pulse width property from the memory module and to generate a new signal based thereon;

wherein the new signal is used instead of the error signal to control the frequency of the voltage controlled oscillator.

13. A computer-readable medium containing a computer program for maintaining a frequency of a voltage controlled oscillator, said program including instructions for executing the steps of:

receiving, at a phase detector, a phase input signal and a phase feedback signal from the voltage controlled oscillator;

measuring a pulse width property of an error signal output from the phase detector to obtain a pulse width property measurement;

storing the pulse width property measurement in a memory; and

generating a new signal based on the stored pulse width property measurement to phase-lock the voltage controlled oscillator.

14. The computer-readable medium of claim 13, wherein said step of measuring a pulse width property measures a duration of a high signal level and a duration of a low signal level of the error signal, and said step of generating a new signal generates a high signal level for a time duration corresponding to the measured high signal level and generates a low signal level for a time duration corresponding to the measured low signal level.

15. A method for calibrating a phase-locked loop, comprising:

receiving an input phase signal and a feedback signal into a phase detector such that the loop is phase-locked;

measuring a pulse width property of an error signal output from the phase detector;

storing the measured pulse width property of the error signal;

using the stored pulse width property to generate a calibration reference signal which can be supplied to the phase detector.

16. A method of implementing clock holdover in a phase-locked loop, comprising:

receiving an input phase signal and a feedback signal into a phase detector such that the loop is phase-locked;

periodically measuring a pulse width property of an error signal output from the phase detector;

determining whether the measured pulse width property satisifies a predetermined condition over a predetermined period of time, and storing the measured pulse width property if it satisfies the predetermined condition;

using the stored pulse width property to generate a reference signal to be supplied to the phase detector when the input phase signal is lost or becomes unsuitable for proper operation of the phase-locked loop.

17. A method of qualifying a potential clock reference for a phase-locked loop, said phase-locked loop comprising a phase detector having a phase input signal and a phase feedback signal as inputs, a system clock and a VCO, said method comprising:

a. determining a relative frequency measurement of the potential clock reference relative to the system clock;

b. measuring a pulse width property of an error signal output from the phase detector;

c. determining a frequency output of the VCO from the measured pulse width property; and

d. determining whether the potential clock reference would lock the phase-locked loop from the determined relative frequency measurement and the determined VCO frequency output.